**Filtro LP Butterworth**

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| **Quantizado 7 bits Forma direta II Second-Order Sections** | |
| --------------------------  Section #1  --------------------------  Quantized Numerator:  1  1.75  6.375  Quantized Denominator:  1  0  0  Quantized Gain:  0.03125  --------------------------  Section #2  --------------------------  Quantized Numerator:  1  2  1  Quantized Denominator:  1  0.34375  0.1875  Quantized Gain:  1  --------------------------  Section #3  --------------------------  Quantized Numerator:  1  0.25  0.125  Quantized Denominator:  1  -0.28125  0.25  Quantized Gain:  1  --------------------------  Section #4  --------------------------  Quantized Numerator:  1  1  1  Quantized Denominator:  1  0.0625  0.75  Quantized Gain:  1  --------------------------  Quantized Output Gain:  1 | --------------------------  Section #1  --------------------------  Reference Numerator:  1  1.728785890470766251070244834409095346928  6.374247613708532433918207971146330237389  Reference Denominator:  1  0  0  Reference Gain:  0.03125  --------------------------  Section #2  --------------------------  Reference Numerator:  1  1.999999999999992894572642398998141288757  0.999999999999999777955395074968691915274  Reference Denominator:  1  0.357130077755224983881987554923398420215  0.176345900779644293443482183647574856877  Reference Gain:  1  --------------------------  Section #3  --------------------------  Reference Numerator:  1  0.271214109529229419059959127480397000909  0.156881260440744491058140397399256471545  Reference Denominator:  1  -0.269508473259425618273610325559275224805  0.240958472709066728878468666152912192047  Reference Gain:  1  --------------------------  Section #4  --------------------------  Reference Numerator:  1  1.000000000000005329070518200751394033432  0.999999999999998556710067987296497449279  Reference Denominator:  1  0.068628395504200134791261689315433613956  0.735431878394071092408523782069096341729  Reference Gain:  1  --------------------------  Reference Output Gain:  1 |

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| **Comparativo** | |
| Discrete-Time IIR Filter (real)  -------------------------------  Filter Structure : Direct-Form II  Numerator Length : 9  Denominator Length: 9  Stable : Yes  Linear Phase : No  Arithmetic : fixed  Numerator : s7,5 -> [-2 2)  Denominator : s7,5 -> [-2 2)  Input : s16,15 -> [-1 1)  Output : s16,9 -> [-64 64)  State : s16,15 -> [-1 1)  Numerator Prod : s23,20 -> [-4 4)  Denominator Prod : s23,20 -> [-4 4)  Numerator Accum : s40,20 -> [-524288 524288)  Denominator Accum : s40,20 -> [-524288 524288)  Round Mode : convergent  Overflow Mode : wrap  Cast Before Sum : true    Implementation Cost  Number of Multipliers : 17  Number of Adders : 16  Number of States : 8  Multiplications per Input Sample: 17  Additions per Input Sample : 16 | Discrete-Time IIR Filter (real)  -------------------------------  Filter Structure : Direct-Form II, Second-Order Sections  Number of Sections : 4  Stable : Yes  Linear Phase : No  Arithmetic : fixed  Numerator : s7,3 -> [-8 8)  Denominator : s7,5 -> [-2 2)  Scale Values : s7,10 -> [-6.250000e-02 6.250000e-02)  Input : s16,15 -> [-1 1)  Section Input : s16,12 -> [-8 8)  Section Output : s16,9 -> [-64 64)  Output : s16,9 -> [-64 64)  State : s16,15 -> [-1 1)  Numerator Prod : s23,18 -> [-16 16)  Denominator Prod : s23,20 -> [-4 4)  Numerator Accum : s40,18 -> [-2097152 2097152)  Denominator Accum : s40,20 -> [-524288 524288)  Round Mode : convergent  Overflow Mode : wrap  Cast Before Sum : true    Implementation Cost  Number of Multipliers : 15  Number of Adders : 14  Number of States : 8  Multiplications per Input Sample : 15  Additions per Input Sample : 14 |

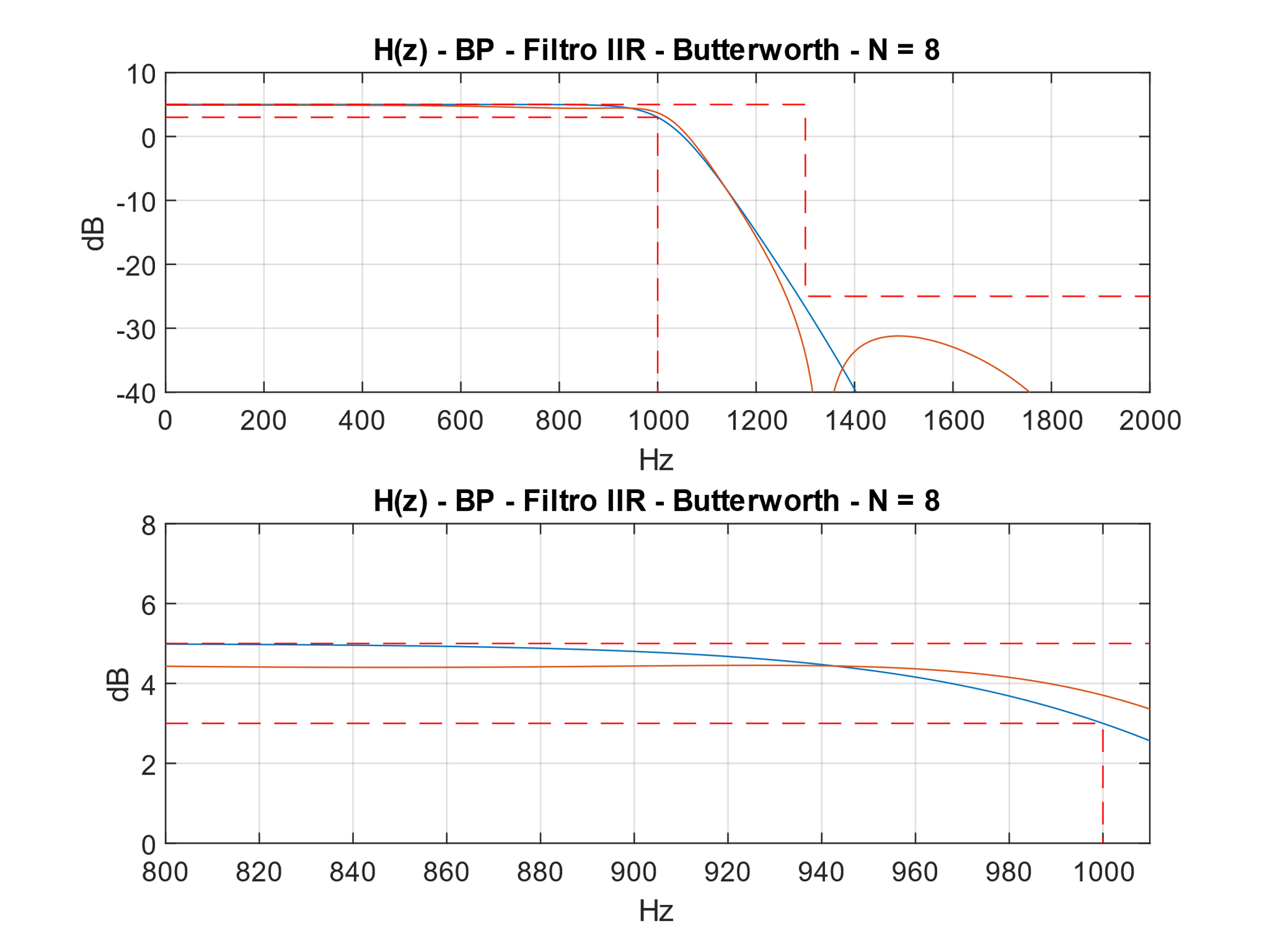


Figura - Filtro DFII

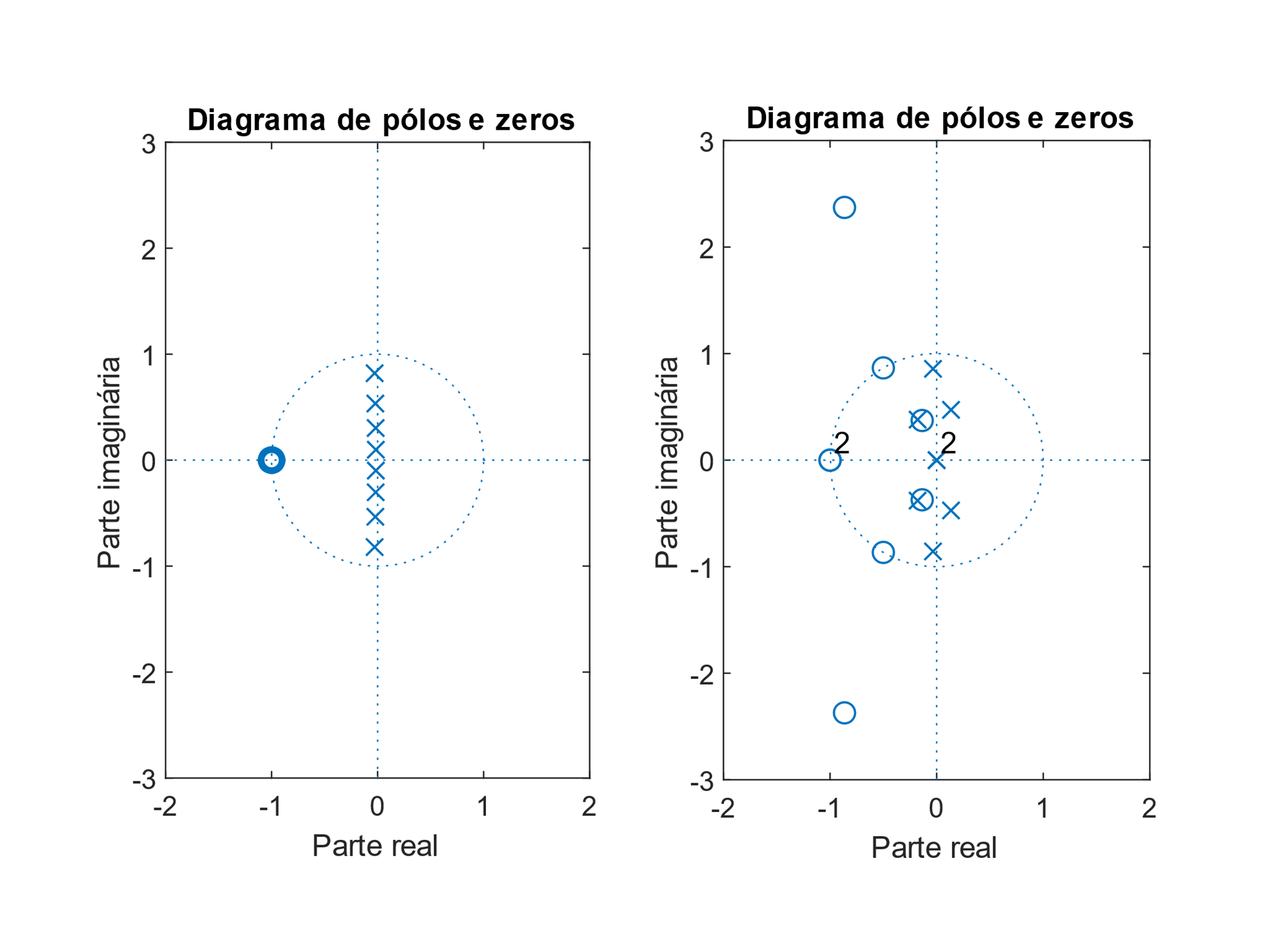


Figura - Filtro DFII

ASIC:

(2M + S + D) \* nº bits

(2 \* 15 + 14 + 8) \* 7 = 364 elementos

FPGA:

(2M + S) \* nº bits

(2 \* 15 + 14) \* 7 = 308 elementos

**Filtro LP Janela Kaiser**

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| **Quantized Numerator 8bits** | **Reference Numerator** | |
| 0.03125  -0.015625  -0.046875  0.0546875  0.0703125  -0.140625  -0.0859375  0.5390625  0.9609375  0.5390625  -0.0859375  -0.140625  0.0703125  0.0546875  -0.046875  -0.015625  0.03125 | 0.027363250134761516602077691118211077992  -0.014327401633311670492432199353061150759  -0.049690007154582764570260877690088818781  0.052234174394811892783163642661747871898  0.072291844505273303300718623631837544963  -0.143149069954147889482953814876964315772  -0.089176737189347057843669119847618276253  0.536803318067287871251380693138344213367  0.961649065426961824343266016512643545866  0.536803318067287871251380693138344213367  -0.089176737189347057843669119847618276253  -0.143149069954147889482953814876964315772  0.072291844505273303300718623631837544963  0.052234174394811892783163642661747871898  -0.049690007154582764570260877690088818781  -0.014327401633311670492432199353061150759  0.027363250134761516602077691118211077992 | |
| **Comparativo** | | |
| Discrete-Time FIR Filter (real)  -------------------------------  Filter Structure: Direct-Form Symmetric FIR  Filter Length : 17  Stable : Yes  Linear Phase : Yes (Type 1)  Arithmetic : fixed  Numerator : s8,7 -> [-1 1)  Input : s16,15 -> [-1 1)  Filter Internals: Full Precision  Output : s25,22 -> [-4 4)(auto determined)  Tap Sum : s17,15 -> [-2 2)(auto determined)  Product : s24,22 -> [-2 2)(auto determined)  Accumulator : s25,22 -> [-4 4)(auto determined)  Round Mode : No rounding  Overflow Mode : No overflow    Implementation Cost  Number of Multipliers : 9  Number of Adders : 17  Number of States : 16  Multiplications per Input Sample : 9  Additions per Input Sample : 17 | | Discrete-Time FIR Filter (real)  -------------------------------  Filter Structure : Direct-Form FIR Transposed  Filter Length : 17  Stable : Yes  Linear Phase : Yes (Type 1)    Implementation Cost  Number of Multipliers : 17  Number of Adders : 16  Number of States : 16  Multiplications per Input Sample : 17  Additions per Input Sample : 16 |

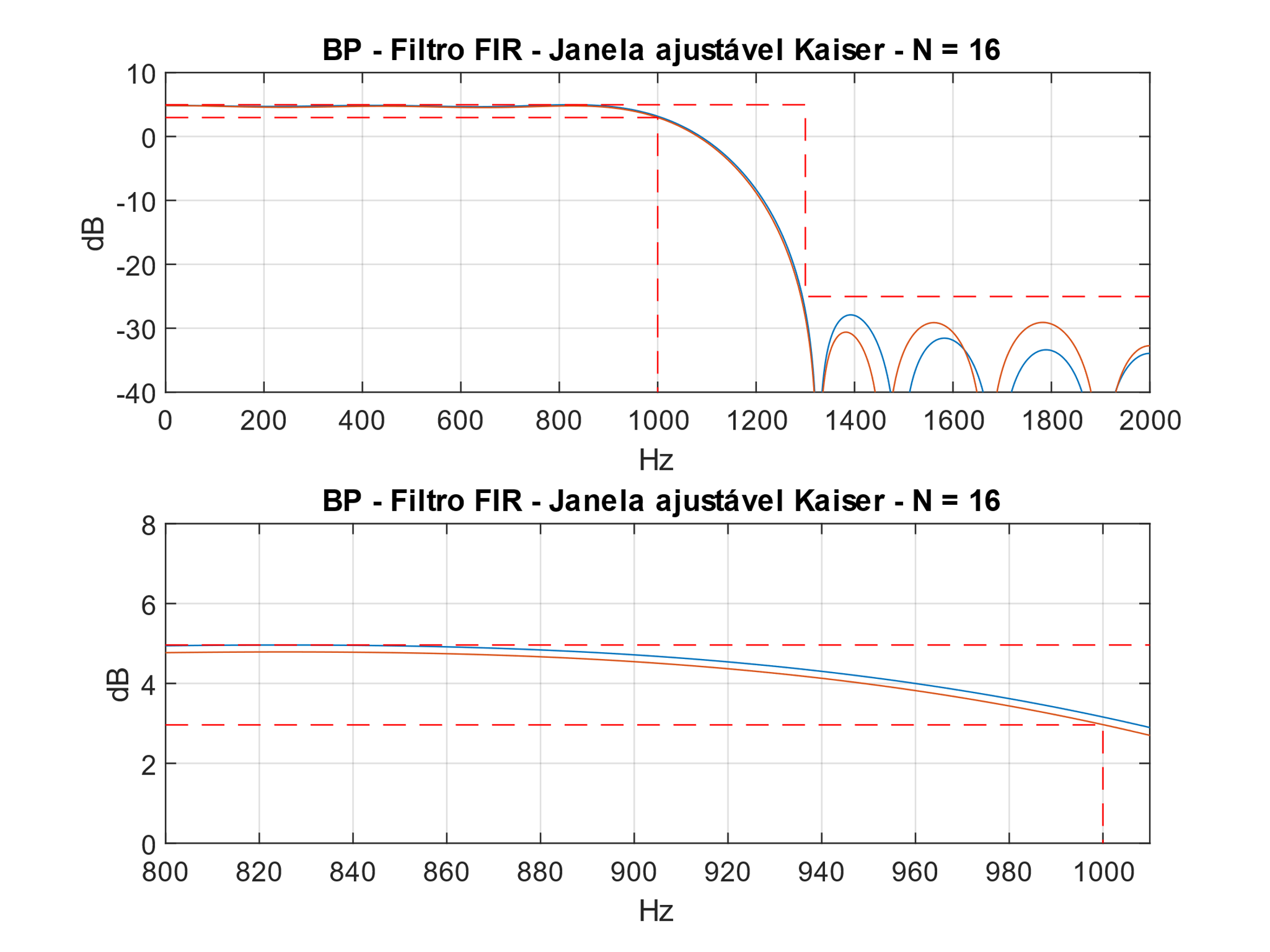


Figura - Filtro DF Symmetric.

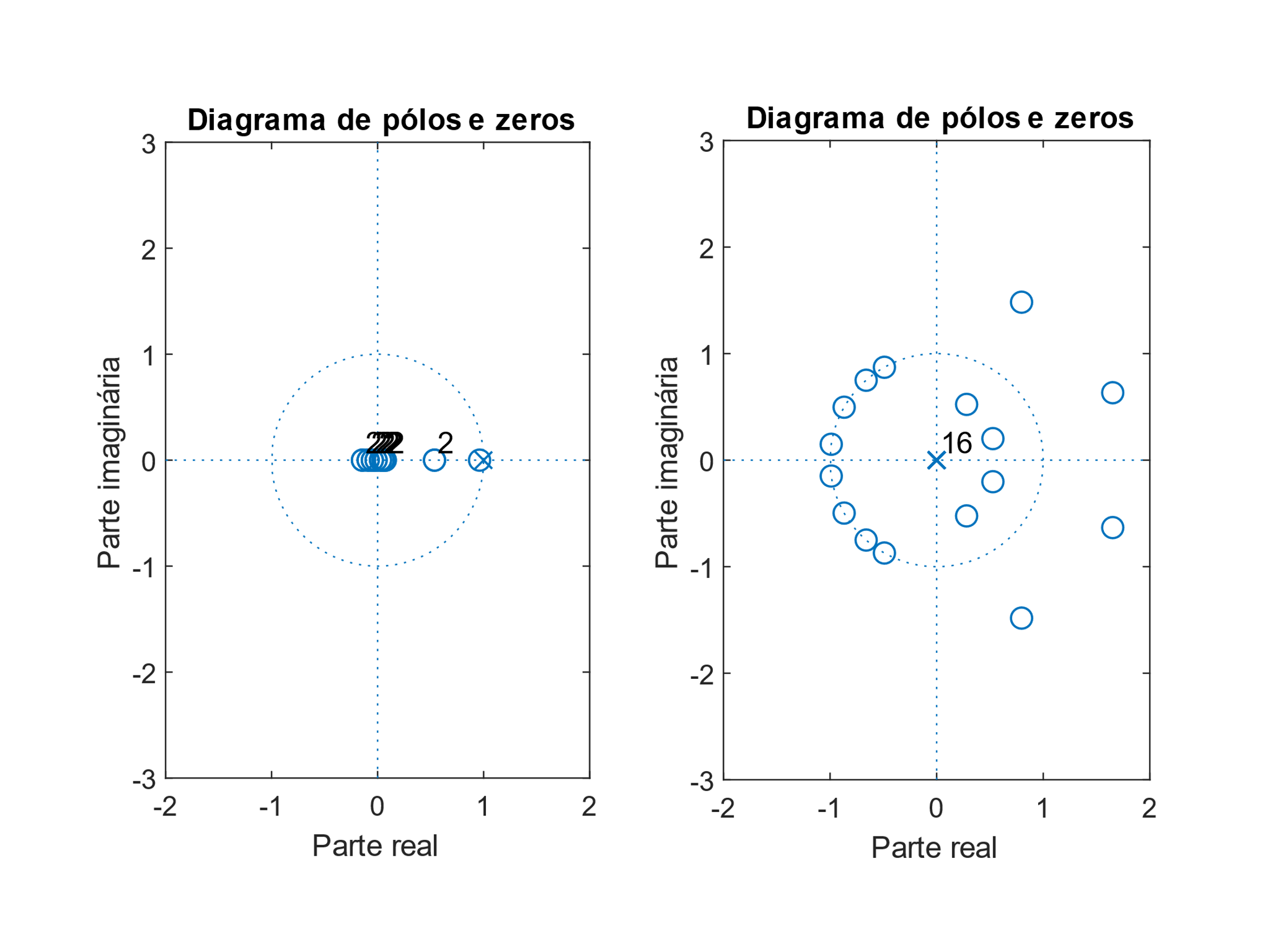


Figura - Filtro DF Symmetric.

ASIC:

(2M + S + D) \* nº bits

(2 \* 9 + 17 + 16) \* 8 = 408 elementos

FPGA:

(2M + S) \* nº bits

(2 \* 9 + 17) \* 8 = 280 elementos